A 3-bit 4th-order Σ-Δ Modulator with Metal-connected Multipliers for Fractional-*N* Frequency Synthesizer

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Abstract — **This paper presents a 3-bit 4th-order Σ-Δ modulator for fractional-*N* frequency synthesizer. The modulator employs an interpolative architecture with multiple feedback paths and metal-connected multipliers to implement the feedback coefficients, resulting in a simple hardware complexity. A frequency synthesizer with the proposed modulator exhibits lower out-of-band phase noise, a frequency resolution of 6-Hz, and fast switching time. The experimental results show –82 dBc/Hz in-band phase noise and –140 dBc/Hz out-of-band phase noise at 1 MHz offset frequency. The fractional spurs are less than –80 dBc. A prototype has been implemented in 0.5-μm BiCMOS technology.**

I. INTRODUCTION

In conventional integer-*N* frequency synthesizer(FS), the comparison frequency of the phase frequency detector(PFD) should be equal to the channel spacing of the synthesizer and there are trade-offs between choosing the loop bandwidth, noise suppression, and spurious tone suppression. To overcome this drawback, a fractional-*N* FS has been chosen. In the fractional-*N* FS, the loop bandwidth is not limited by the channel spacing, because the comparison frequency of the PFD can be increased independently without affecting the channel spacing[1]. The generation of unwanted fractional spurs, in addition to the reference spurs, is the fundamental problem of the fractional-*N* FS. Among many methods to suppress fractional spurs, a Σ-Δ modulation technique using an over-sampling principle has shown a desirable performance in previous literatures[2][3].

The fractional-*N* FSs using the Σ-Δ modulator, however, have several problems such as idle-tones and unsuppressed out-of-band phase noise of the PLL around the corner-frequency of the modulator. In Fig. 1, the phase noise contribution of the Σ-Δ modulator in fractional-*N* FSs is shown. We can find the phase noise of the modulator dominates that from other noise sources and deteriorates the out-of-band phase noise of the PLLs. Multi-bit modulators can push up the corner frequency to higher frequency and relieve the phase noise boosting.

In this work, we propose a 3-bit 4th-order Σ-Δ modulator, which is free from out-of-band phase noise degradation caused by the Σ-Δ modulator and offers a good idle-tone performance without dithering. The feedback coefficients of the modulator are realized using metal-connected multipliers without increasing the hardware complexity compared with that of single-bit.

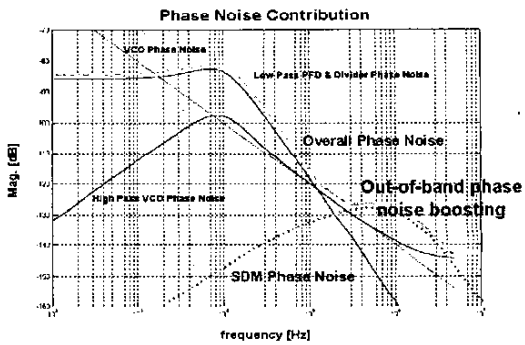

Fig. 1. Overall phase noise contributions of Σ-Δ frequency synthesizers.

II. FRACTIONAL-*N* FREQUENCY SYNTHESIZER

A block diagram of the fractional-*N* FS is illustrated in Fig. 2. The synthesizer consists of a dual modulus prescaler, a PFD, a charge-pump, a Σ-Δ modulator, a serial data control block, and a programmable *N*-counter with an external LPF and a voltage controlled oscillator.

The programmable *N*-counter determines the final division ratio of the prescaler dynamically by combining the output of the serial data control block with the output of the modulator to serve as a multi-modulus divider. The phase detector is composed of a PFD and a charge-pump. The charge-pump provides current into an external loop filter in proportional to the phase difference between two input signals of the PFD. In the multi-bit modulator, the linearity of the PFD is very important, because the folding-in noise of the modulator degrades the in-band phase noise and limits spurious tones performance. As the

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dead-zone problem is caused by the insufficient turn-on time of the charge-pump, a dead-zone free PFD providing an additional delay is used to prevent non-linearity error around 0° phase difference in the locked condition.

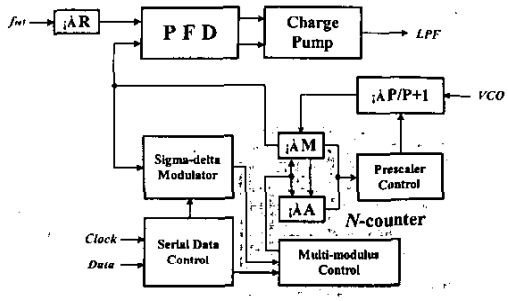


Fig. 2. The architecture of the fractional-*N* FS.

1. 3-bit 4th-order Σ-Δ Modulator

There are two types of noise shaping architectures - interpolative type and MASH type. The MASH architecture is unconditionally stable, but its architecture is complicated, and each stage should have its own independent dither to provide the most uncorrelation of the quantization error and tends to generate wide-spread high-frequency bit patterns resulting in more folding-in noise within the band[4].

An interpolative Σ-Δ modulator is very simple and generates less high-frequency noise, but the full input range is not allowed because of its stability requirements. This limitation in the full input range causes the dead-band problem that is a barrier to the single-bit interpolative architecture[4]. In general, Butterworth filter coefficients are used to limit the pass-band gain level of the noise transfer function because of nonlinear stability. But there is a trade-off between the pass-band gain of the noise transfer function and the corner frequency of the modulator (Fig. 3). If the corner-frequency is increased, the pass-band gain level also increases. In other words, once the pass-band gain level is chosen, the corner-frequency of modulator is also determined[4].

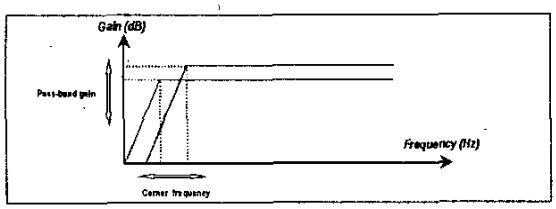


Fig. 3. Trade-off between the pass-band gain and the corner-frequency of the Σ-Δ modulator.

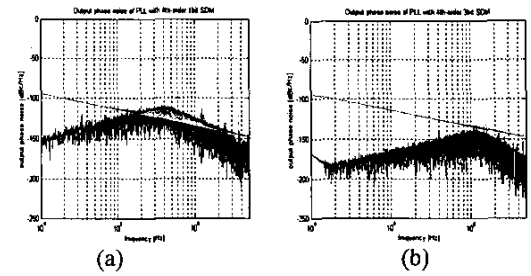
Table 1. shows the number of quantizer levels and corresponding maximum allowable corner frequency[4]. The maximum corner frequency of the single-bit and the 3-bit modulators are around 0.06**fs* and 0.19**fs* respectively.

Table 1. Number of quantizer levels and Maximum allowable corner frequency.

Number of quantizer levels	Maximum pass-band gain	Corresponding corner frequency
2	1.5	0.06fs
4	2.5	0.13fs
8	3.5	0.19fs

(where fs is the operating frequency of the modulator)

Fig. 4 shows the outputs of the PLL of a single-bit and a multi-bit modulators when the operating frequency of the modulator is 9.84MHz. The diagonal line indicates the out-of-band phase noise of the external VCO. As shown in Fig. 4(a), the low corner frequency of the single-bit modulator gives a rise to a serious problem on out-of-band phase noise of the PLL. A multi-bit quantizer, on the other hand, provides high spectral purity by reducing quantization noise itself and can increase the corner frequency further[5]. Fig. 4(b) shows the improved out-of-band phase noise of the synthesizer with a multi-bit architecture.



(a) (b)

Fig. 4. Out-of-band Phase Noise of PLL with a single -bit modulator (a) and multi-bit modulator (b). (*fs* =9.84MHz, *fvco* =979.35MHz)

To obtain better idle-tone performance, the output bit-patterns should be randomized. A single-bit architecture with dithering, increasing the order of the modulator, and a multi-bit quantizer are preferred choices. A 3-bit 4th-order modulator showed a good idle-tone property without dithering. Since the discrete Fourier transform does not provide true power spectrum, when the signal is aperiodic or random[4], the autocorrelation estimation was used to see the randomness of the output sequences.

The proposed 3-bit 4th-order Σ-Δ modulator with an 8-level quantizer and multiple feedback paths is shown in Fig. 5. Each stage consists of an adder, an accumulator, a

multiplier for the dynamic scaling, and metal-connected multiplier to realize feedback coefficients. Each stage has 8 feedback coefficients, and totally 32 feedback coefficients are in used. In the final stage, the output data of the modulator are quantized and decoded into 3-bit gray-coded data. The control signal generation block generates basic 8 control signals, and the signals are fed back to the each stage. Metal-connected multipliers arrange the generated signals to realize feedback coefficients. There are no linearity problems with the modulator because the modulated data are conveyed in the full digital domain. The input range of the modulator is 1/8 of the full range, and the fractional division ratio is 1/1560096 (–780048 ~ 780048) resulting in less than 10Hz frequency resolution with 9.84MHz comparison frequency. Since the modulator is implemented based on the two's complement binary system, the output data of the modulator have 8 levels from –4 to +3. The stability problem was verified with Matlab simulations.

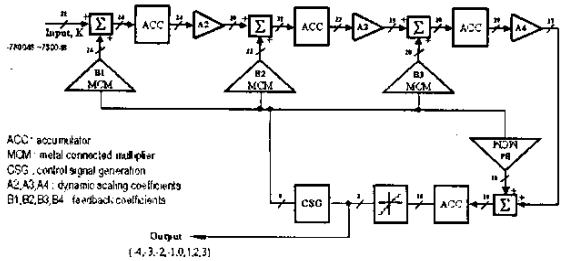


Fig. 5. 3-bit 4[th] -order Σ-Δ modulator.

2. Metal-connected Multiplier

As there are multiple paths in the modulator and each path has 8 coefficients depending on the output data, it is not easy to implement the feedback coefficients without excess hardware complexity. The proposed modulator has 4 stages - 24bit, 22bit, 20bit, and 18bit. If we consider ROM-based multipliers, approximately 720bit (90bit x 8) storage would be needed. In this work, a simple decoding of the modulator output data makes it possible to implement the feedback coefficients with metal-connected multipliers. If we convert the two LSBs of the modulator output to gray-coded data, which have a symmetric property, all the possible feedback coefficients can be implemented by using several control signals generated from the output of the modulator.

To minimize hardware complexity the number of the control signals should be minimized. Fig. 6 shows an example of 20bit feedback coefficients in a stage. There are two bit group(BG)s. BG1~BG4 have constant values and the others have variable values. The groups with constant values are easy to implement with supply and ground signals. Although the number of the groups with variable values are 256, only 16 control signals are enough with gray-coded data because of their symmetric property. Final control signals are just 8 as shown in Fig. 6. Basic 8 signals and the inverted 8 signals are used to realize feedback coefficients. The inter-stage scaling coefficients for dynamic scaling are set to be the power of 2 to realize multipliers with shift operations.

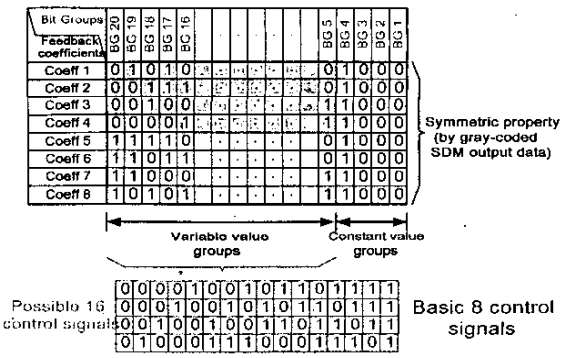


Fig. 6. Principle of the control signal generation.

III. EXPERIMENTAL RESULTS

The fractional-*N* FS has been implemented in a 0.5-μm 15-GHz BiCMOS technology. To verify the synthesizer performances with the modulator, a 20-kHz bandwidth PLL loop, an external 27-MHz/V VCO, a 3[rd] order passive LPF, a 600-μA charge-pump current, and 9.84-MHz PFD comparison frequency were used.

Fig. 7 shows that the phase noise of the 985.18-MHz carrier frequency is –140 dBc/Hz at 1-MHz offset. The in-band phase noise is –82 dBc/Hz. A reference spur of less than –80 dBc and a fractional spur of less than –80 dBc are observed. The measured lock time is less than 0.5 ms. In Fig. 7 and Fig. 8, we can see the out-of-band phase noise degradation has been disappeared in the case of 3-bit modulator. The measured results of the FS are summarized in Table 2 and meet all requirements for CDMA applications.

Fig. 9 shows the microphotograph of the multi-bit and the single-bit modulators. Single-bit modulator has 4 stages - 21bit, 18bit, 15bit, and 11bit. Taking into account the increased number of bit in each stage, the hardware complexity of the multi-bit modulator is almost the same as that of the single bit.

IV. CONCLUSION

In this paper, multi-bit and single-bit modulators are compared. Although multi-bit modulator has many advantages, the increased hardware complexity was a burden in multi-bit modulator design. We proposed a 3-bit 4^{th}-order Σ-Δ modulator, which is free from out-of-band phase noise degradation caused by the Σ-Δ modulator, and introduced simple metal-connected multipliers to realize the feedback coefficients.

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Table 2. Measurement results of the Frequency Synthesizer. *(fpfd =9.84MHz, fvco=985.18MHz)*

Supply voltage	3 V
Current consumption	5.5 mA
Max. output frequency	2.5 GHz
Min. frequency resolution	6 Hz
Lock time	500 μs
In-band phase noise	-82 dBc/Hz
Out-of-band phase noise @ 1 MHz	-140 dBc/Hz
Reference spur	-75 dBc/Hz
Fractional spur @ 200 KHz	< -80 dBc/Hz

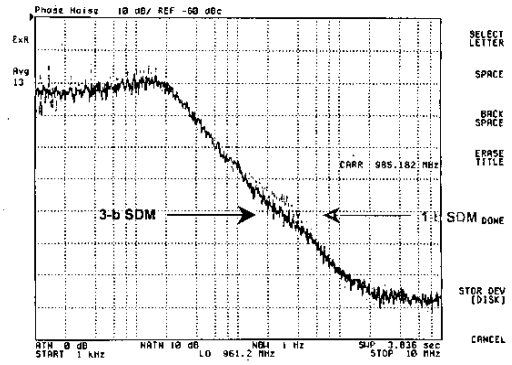

Fig. 7. Measured phase noise at 985.18MHz. (.F= 0.623)

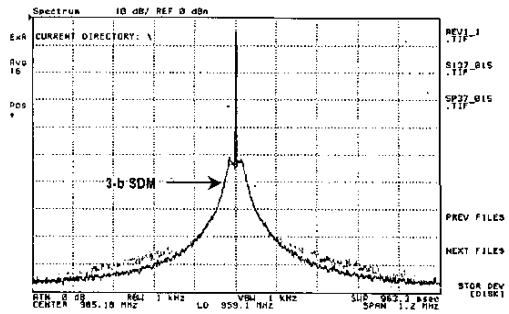

Fig. 8. Measured output spectrum at 959.1MHz. (.F= 0.906)

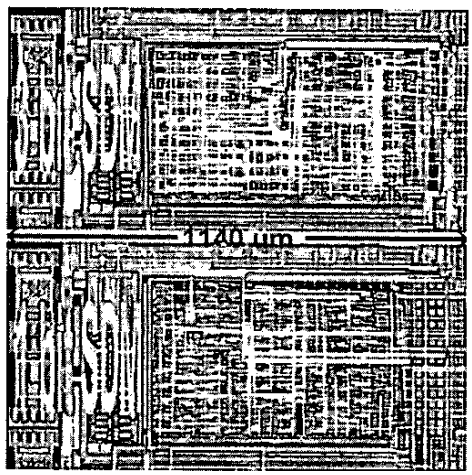

Fig. 9. Chip photograph of the multi-bit and the single-bit modulators.